REMARKS

Pursuant to the present amendment, claims 1, 6-8, 22, 30, 32, 35, 37 and 40 have been amended and claims 23-25 have been canceled. Thus, claims 1-9, 22 and 26-41 are pending in the present application. No new matter has been introduced by way of the present amendment. Reconsideration of the application is respectfully requested.

As an initial matter, claims 6-8 were rejected under 35 U.S.C. § 112. Pursuant to the present amendment, claims 6-8 have been amended in a manner believed to provide the proper antecedent basis as requested by the Examiner with respect to these claims. Withdrawal of the Section 112 rejection is respectfully requested.

In the Office Actions, claims 1-5, 7-8, 22-23, 26-28 and 30-31 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Ishida (U.S. Patent No. 6,344,396). Claims 1-3, 7, 22-23 and 25-31 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Long (U.S. Patent No. 6,153,534). Claims 6, 24-25 and 32-41 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Ishida or Long in view of Iyer (U.S. Patent No. 6,121,133). Applicants respectfully traverse the Examiner's rejections.

As the Examiner well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App. & Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should

have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. "Inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office's burden of establishing prima facie anticipation includes the burden of providing "...some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Skinner* at 1789.

Moreover, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Pursuant to the present amendment, independent claim 1 has been amended to recite the steps of depositing a first layer above the surface of the substrate, depositing a second layer of material on the first layer and, after depositing the first layer and the second layer of material, patterning the second layer of material and the first layer to form a semiconductor device feature in the first layer. As amended, it is respectfully submitted that independent claim 1 is allowable over the prior art of record.

Ishida is understood to be directed to a method of forming asymmetrically configured transistors using a technique involving removable sidewall spacers. Abstract. To that end, Ishida discloses the deposition of a layer of dielectric material 14 over a pre-existing gate electrode structure comprised of a gate dielectric layer 11, a gate electrode layer 12, and first or

inner sidewall spacers 13. Figure 1(B); Col. 10, ll. 16-66. Thereafter, as shown in Figure 1(C), an anisotropic etching process is performed to form sidewall spacers 14 adjacent the previous gate electrode structure. Then, a photoresist masking layer is formed so as to cover approximately half of the gate electrode structure and one of the spacers 14'. Figure 1(D); Col. 11, ll. 31-39. The exposed sidewall spacer pair 13, 14' is then subjected to an ion implantation process 15A to change the etching characteristics of the spacer.

Long is understood to be directed to a method of fabricating a dual material gate of a field effect transistor. Col. 2, ll. 27-42. In the cited portions of Long identified by the Examiner, a spacer dielectric layer 250 is formed over an anti-reflective coating (BARC) layer 216 that remains positioned on top of the first material gate portion 214. Figures 5A-5B; Col. 5, ll. 33-42. Next, as indicated in Figures 6A-6B, heavy ions are implanted into the spacer dielectric layer 250 wherein the implantation process is performed at an angle such that the heavy ions are substantially not implanted into the drain side 220 of the devices. Col. 5, ll. 44-52. The purpose of the implantation process is to enhance the etch rate of the portions of the spacer dielectric layer 250 that are implanted with the heavy ions. Col. 5, l. 66 – Col. 6, l. 11. After the angled implant process is performed, the spacer dielectric layer 250 is selectively etched such that the spacer dielectric layer 250 is etched from the top of the BARC layer 216 and the source side 218 of the first material gate portion 214 while the spacer dielectric 250 is substantially not etched from the drain side 220 of the first material gate portion 224. Col. 5, ll. 58-65.

With this understanding of the Examiner's two primary references, it is respectfully submitted that all pending claims are in condition for immediate allowance. For example, amended independent claim 1 specifically recites the step of, after depositing the first layer and the second layer of material, patterning the second layer of material and the first layer to form the

semiconductor device feature in the first layer. At no point is the entirety of amended independent claim 1, including the limitation discussed above, disclosed or even remotely suggested in Ishida or Long. In both of those references, a semiconductor device feature has already been formed in the underlying first layer **prior to** the deposition of the second layer identified by the Examiner, *i.e.*, the layer 14 in Ishida and the layer 250 in Long. Thus, neither Ishida nor Long anticipate amended independent claim 1.

Moreover, there is no suggestion in either Ishida or Long, or any other art of record, to modify the teachings of those references so as to arrive at Applicants' claimed invention. In Ishida there is simply no suggestion for the steps of depositing first and second layers and implanting ions into the second layer of material to modify a structure of the material of the second layer and, after depositing the first and second layers, patterning the second layer of material and the first layer of material to form a semiconductor device feature in the first layer. Ishida is simply directed to a technique whereby one of the sidewall spacers positioned adjacent the gate electrode structure disclosed therein may be selectively exposed to an ion implantation process so as to effect the etching characteristics of the exposed sidewall spacer. The technique disclosed therein is primarily employed in the formation of asymmetric semiconductor devices.

Long is similarly deficient. Long is directed to making a gate electrode comprised of two different materials. To that end, Long discloses a process flow wherein an angled ion implantation process is effectively employed to enable the removal of what would otherwise be sidewall spacer material from above the source side 218 of the device. Thereafter, with the spacer dielectric layer 250 asymmetrically covering only the drain side 220 of the gate portion 214, a second material gate portion 260 is selectively grown on the exposed source side 218 of the gate portion 214. Figures 8A-8B; Col. 6, ll. 23-32. Again, there is simply no suggestion in

Long to modify the teachings therein so as to arrive at Applicants' claimed invention wherein ions are implanted into the second layer of material to effect the etching characteristics thereof and, after the first and second layers of material are deposited, an etching process is performed to form a semiconductor device feature in the underlying first layer of material.

The Examiner's citation to Iyer for the proposition silicon nitride or silicon oxide can act as an anti-reflective coating layer is simply not relevant to the fundamental deficiencies set forth in the Examiner's primary references of Ishida and Long.

It is respectfully submitted that any attempt to assert that the invention defined by amended independent claim 1 is obvious in view of Ishida or Long considered individually or collectively, in addition to any other prior art of record, constitutes an improper use of hindsight using Applicants' disclosure as a roadmap. A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. Accordingly, it is respectfully submitted that amended independent claim 1, and all claims depending therefrom, are in condition for immediate allowance.

Pursuant to the present amendment, independent claims 22, 32 and 37 have been amended to recite that the first layer of material comprises a gate electrode material and the second layer of material comprises anti-reflective coating material. Moreover, all of these independent claims have been amended to recite that the implantation step is performed after the first and second layers of material are formed. As thus amended, it is respectfully submitted that

independent claims 22, 32 and 37, as well as all claims depending therefrom, are in condition for immediate allowance. As describe above, neither Ishida nor Long disclose or even remotely suggest a methodology wherein a layer of gate electrode material is depositing, a layer of anti-reflective coating material is then deposited on the layer of gate electrode material, and, after the formation of both those layers, an ion implantation process is performed to modify the structure of the anti-reflective coating material. Ishida does not specifically disclose or discuss that a BARC layer is formed above the gate electrode layer 12 disclosed therein. However, such methodologies are well known in the art. Nevertheless, there is certainly no suggestion or disclosure in Ishida that an ion implantation process should be performed on the anti-reflective coating layer to change the etching characteristics of that layer. As described above, Ishida is simply directed to a process of forming an asymmetrically configured transistor. To achieve that goal, the process disclosed therein provides means for selectively implanting ions into an exposed spacer pair to enhance the etching characteristics of that exposed spacer pair.

Although Long discloses the formation of a BARC layer 216 above the first gate portion 214, at no point does Long disclose or even remotely suggest performing an ion implantation process to change the etch selectivity of the layer 216. Long is simply directed to changing the etch selectivity of the layer 250 on the source side of the devices disclosed therein such that the portions of the layer on the source side may be removed to allow for the formation of a second material portion of the gate 260. Again, there is not the slightest suggestion that an ion implantation process is performed on the BARC layer 216 disclosed in Long. If anything, Long could be said to teach away from the present invention in that, although the BARC layer is present, there is not even the slightest suggestion that an implantation should be performed on that layer to modify the etching characteristics of the BARC layer 216.

Amended dependent claims 30, 35 and 40 are likewise believed to be allowable for independent reasons. These dependent claims recite the step of, after implanting the ions, performing at least one etch process to define a feature in the first layer of material, *i.e.*, the layer of gate electrode material. As amended, it is respectfully submitted that dependent claims 30, 35 and 40 are independently allowable over the art of record. In addition to the detailed steps set forth in each of their respective independent claims, neither of the primary references identified by the Examiner disclose the concept of waiting until after the ion implantation process is performed into the anti-reflective coating material to perform an etching process to define a feature in the gate electrode material layer. Accordingly, it is respectfully submitted that these dependent claims are allowable for independent reasons.

In view of the foregoing, it is respectfully submitted that all pending claims are in condition for immediate allowance. The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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